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Review Literature for Mosfet Devices Using High-K

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Abstract: ***With the advancement of MOS devices over 40 years ago, SiO_2 has been used as an efficient gate dielectric. The need for increased speed at constant power density has led to shrinking of MOSFET dimensions and as per scaling rules; the oxide thickness is also reduced in step. With scaling reaching sub nanometer technology nodes, the introduction of novel materials became inevitable as scaling of SiO_2 raises a serious concern in terms of tunneling current and oxide breakdown. High-k gate technology is emerging as a strong alternative for replacing the conventional SiO_2 dielectrics gates in scaled MOSFETs for both high performance and low power applications. High-k oxides offer a solution to leakage problems that occur as gate oxide thickness' are scaled down. Therefore, it is necessary to replace the SiO_2 with a thicker layer of higher dielectric constant. Considering scaling issues various criteria of selection of dielectric and detailed study of various dielectrics are studied in this paper. Since high-k dielectric is not as favorable as the native oxide (SiO_2) some factors need to be considered while replacing SiO_2 by other dielectric materials.***

Keywords: Dielectric, High-k, Material oxides, Scaling.

1. INTRODUCTION

With the advance of metal oxide semiconductor technology, Si based semiconductors, with SiO_2 as an outstanding dielectric, have been dominating microelectronic industry for decades. As per G.Moore, with the advent of MOS devices over 40 years ago, SiO_2 has been used as an efficient gate dielectric. The need for increased speed at constant power density has led to shrinking of MOSFET dimensions and as per scaling rules; the oxide thickness is also reduced in steps [4].

In the current version of the International Technology Roadmap for Semiconductors (ITRS), the scaling of the metal-oxide-semiconductor field-effect transistor (MOSFET) is projected to the year 2016 when the channel length should be 9 nm as shown in Figure 1 [1]. Recently, some semiconductor companies have moved to the leading-edge of the 32 nm technology node and successfully realized advanced product development. Presently companies are continuing research and development the 22 nm and beyond complementary metal oxide semiconductor (CMOS) technology [4]. Oxide materials with large dielectric constants (so-called high-*k* dielectrics) have attracted much attention due to their potential use as gate dielectrics in MOSFETs [2].

When the channel length becomes of the same order of magnitude as the depletion-layer widths of the source and drain, a MOSFET device is considered to be short and the so-called short-channel effects arise. To offset short channel effects, the thickness of the gate oxide must be reduced. This causes a reduction in the on/off current ratios. Moreover, the reduction of oxide thicknesses results in increased gate leakage current, which is a formidable problem, particularly for large density circuits. The presence of the C_{inv} inherent in the dielectric/semiconductor interface is expected to result in a 30% reduction of the total gate capacitance of high-*k* gate stacks with 1-nm equivalent oxide thickness (EOT). It is required to keep high capacitance density for channel formation in the sub-micron MOSFET with ultra thin SiO_2 layer [5]. The recent trend shows that the high leakage current will prevent the scaling of the SiO_2 below 1nm for future applications. Therefore, thickness reduction of SiO_2 gate layer below 1nm is a big challenge. Again defects are formed in the gate oxide at the SiO_2/Si interface due to flow of charge carriers. If defect density reaches a certain threshold, this may cause quasi-breakdown on the gate layer. This is an important reliability issue of the transistor.

1.1 Scaling Issue of CMOS circuits

Most important research paper which specifies the research required to continue rapid development in semiconductor industry is International Technology Roadmap for Semiconductor (ITRS).

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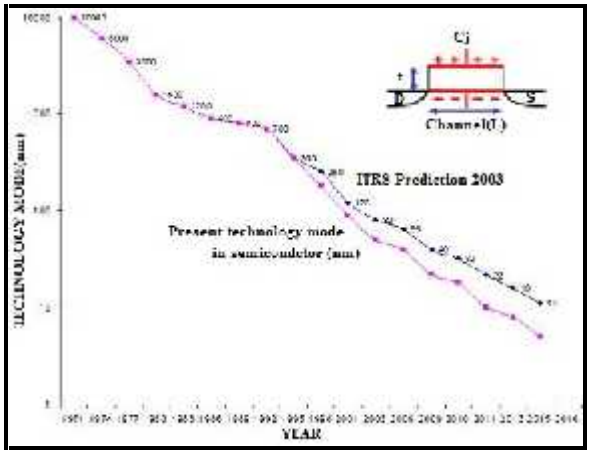

Fig-1 MOS channel length scaling and predication made by ITRS 2003 (blue line) and physical channel length (pink line)

The scaling dimensions have reduced to a factor 1000 during last 40 years (fig-1[4]). The constraint for technology to scale insist that the total power consumption per unit area remains constant which means that as density of the circuitry in a technology increases, the amount of cooling requirement for the circuit remains constant- if this was allowed to increase after some point, the circuit would melts. Many limitations for the down scaling have been proposed in the literature Table1 [3]. The thickness of gate silicon dioxide reaches its thinnest limit. Table-1 The scaling rule for device parameter by a unit less scaling factor á with possible solution for smarter, faster, lower power dissipation, and lower cost IC.

Now further scaling oxide layer is not capable to maintain insulating property, since direct tunneling dominates the leakage current further down scaling leads several physical and technological limitations.

Table -1: Scaling rules.

Parameter	Scaling Factor	Limiting factor	Solutions
Voltage (V_{dd})	1/â	Thermal Voltage/ quantum confinement	Low operating temp.
Electric Field (E)	1	-	-
Channel Length (L)	1/â	Lithography	Double Gate structure

1.2 Current Issue in scaling

The ITRS is most important industrial strategy paper for semiconductor devices & technology towards high performance and lower cost. ITRS is organized by the Semiconductor association of Europe, Japan, Korea, Taiwan and the USA. The representative from leading semiconductor companies around the world agrees on several issues one of them was physical gate length of microprocessor. Currently the International Technology Working Groups (ITWG) USA is responsible for technologies and methodologies used for future area of research.

The National Technology Roadmap of semiconductor (NTRS) and ITRS have scaling predication from 100 components per IC in 1965 to 15 billion in the current state of art. There are less gain in device performance i.e. power consumption, short channel effects and parasitic capacitance as scaling goes further below sub-100 nm. In 2007 the use of high-k dielectrics is introduced for the first time, to address gate leakage issues [3].

The performance of MOS transistor below 30 nm in still below satisfactory and also the characteristics across wafer is also of great concern.

Table -2 Gate dielectric layer technology requirement.
* EOT- equivalent oxide thickness.

Technology Node (nm)	Starting Year	T_{inv} (nm)	*EOT(nm)
45	2007	14	1.0
35	2009	12	0.8
22	2011 2012	10	0.6
16	2013 2014	?	?

Because of downscaling the gate length and gate oxide thickness decreased only 100, supply voltage decreased by factor 10, chip area increased by 10 and power dissipation increased by 10^5, which may not increased under ideal scaling. The major difficulties are tremendous cost of lithography and in developing new technologies. In table-2 column 1 shows technology node which means the smallest poly-Si/metal gate length and column 2 shows expected starting year. It is being noted that neither 22 nm nor 16 nm numerical value appearing

value in the corresponding ITRS parameter sets. The device less than 10nm gate length would be extremely sensitive to the device physical dimensions and variations in material composition. Recently 2009-2010 Intel corporation manufacturing transistors have set a record I_{on} /I_{off} characteristic with different metal gates and high-k dielectric material [3].

2. DESIRABLE CRITERIA of HIGH-K DIELECTRIC

With the scaling of the MOS-device suffers some unsolvable issues. Therefore, it is necessary to replace the SiO_2 with a thicker layer of higher dielectric constant. Since high-k dielectric is not as favorable as the native oxide (SiO_2) some factors need to be considered while replacing SiO_2 by other dielectric materials [6].

2.1 Equivalent Oxide Thickness

EOT is defined as the thickness of SiO_2 layer that would be required to achieve the same capacitance density (capacitance per unit area) as the high-k material in consideration and is given by

$$\frac{D_{eq}}{\varepsilon_{r,sio2}} = \frac{D_{high-k}}{\varepsilon_{r,high-k}} \qquad (1)$$

Further scaling of MOS device is possible if smaller EOT (D_{eq}) can be achieved by using a thicker high-k dielectric layer. However an ultrathin low-k interfacial layer forms either during the deposition of the high-k dielectric or during post-deposition annealing processes [6].

This low-k layer (Fig. 4) will act as a series capacitance and the total capacitance C_{tot} will be

$$\frac{1}{C_{tot}} = \frac{1}{C_{low-k}} + \frac{1}{C_{high-k}} \qquad (2)$$

Then the EOT will be

$$D_{eq} = \left(\frac{\varepsilon_{r,sio2}}{\varepsilon_{r,low-k}}\right) D_{low-k} + \left(\frac{\varepsilon_{r,sio2}}{\varepsilon_{r,high-k}}\right) D_{high-k} \qquad (3)$$

Therefore, EOT is increased due to the presence of the low-k interfacial layer. A suitable alternative high-k gate dielectric has to be found to meet the equivalent oxide thickness (EOT) required by the ITRS [6].

2.2 Energy Band Gap, Permittivity, and Barrier Height

The band-gap of the high-k material decreases with the increase of the permittivity which is given by

$$E_g \approx 20\left[\frac{3}{(2+\varepsilon)}\right]^2 \qquad (4)$$

A small energy band gap causes a small barrier height for the tunneling process in the MOSFETs. Fig. 3 [6] shows the energy band diagram of MOS at equilibrium. Φ_{Be} is the potential barrier between the gate and dielectric oxide when electrons travel from gate to Si substrate and ΔE_c is the barrier height when electrons travel from the Si substrate to the gate,

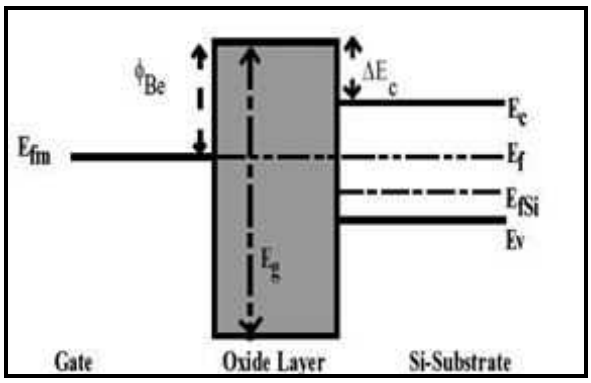

Fig -2: Energy band diagram of MOS transistor.

Small band-gaps are undesirable as leakage current increases with decreasing barrier height and thickness according to the following equation [6]

$$J_{Leakage} \propto \frac{1}{d^2} e^{\left(-\frac{4\pi d}{h}\sqrt{mq2\phi_{Be}-V}\right)} \qquad (5)$$

In equation 5, V is the voltage drop across the dielectric, m is the electron effective mass and d is the thickness of the dielectric. Therefore, to obtain low leakage currents, a gate dielectric with a large band gap is desirable [6].

2.3 Thermodynamic Stability

The interface between ultra thin gate dielectric with Si plays a key role in determining the electrical properties of MOSFETs. The oxide may react with Si and form either SiO_2 or a silicide according to the following reactions [6],

$$MO_2 + Si = M + SiO_2$$
$$MO_2 + 2Si = MSi + SiO_2$$

As explained earlier this SiO_2 will add as a series capacitance which increases the EOT and negates the effect of high-k dielectric. Moreover metal silicide would short out the field effect. Therefore, it is required to use either a high-k gate dielectric material with a good thermodynamic stability on Si or an ultrathin high-k interfacial blocking layer between the gate oxide and Si to avoid the formation of silicide and SiO2. It has been reported that the thermodynamic stability issue may restricts the possible candidates for suitable high-k material from Group II and IV (e.g. SrO, ZrO_2, HfO_2, CaO, BaO, Al_2O_3, Y_2O_3, La_2O_3 and the lanthanides)

2.4 Alloy Crystallization

A polycrystalline gate dielectric suffers a high leakage current due to its grain boundary and affects the device scaling. Moreover, polycrystalline films may cause a non-uniform dielectric property due to variation in the grain size and crystal orientation [5]. Replacing polycrystalline gate oxide by crystalline dielectric is a possibility.

However, some high-k candidates such as HfO_2, ZrO_2 crystallize at a very low temperature of 500^{o}C. Among the other candidate of high-k gate oxide, amorphous Al_2O_3 shows good stability at high temperature however it does not have sufficient high dielectric constant.

2.5 Alloy Crystallization

The gate oxide should not diffuse in the Si-channel or in the gate electrode as well as it should block the penetration of gate electrode components into the channel. Therefore, dielectric oxide with low atomic diffusion coefficient is required. Oxygen diffusion rate can be reduced by alloying with the SiO_2 as Si is covalently bonded to oxygen in silicates. Nitrogen incorporation blocks boron diffusion which also increases the crystallization temperature of the high-k oxides [5].

2.6 High Quality Interface

High quality interface between the high-k gate oxide and the Si is an important selection criterion for alternative dielectrics. The interface between SiO_2/Si offers the best interface quality with the lowest interface state, $D_{it} \sim 10^{10}$ $eV^{-1}cm^{-2}$ [5].

3 MATERIAL USED FOR GATE DIELECTRIC

The choice of thicker class of materials, known as "high-k," may replace today's silicon dioxide technology not for 45 nm or 32 nm but can also be scaled to the end-of-the roadmap technology nodes. Typically for high-k materials under investigation are Al_2O_3, ZrO_2, HfO_2, Ta_2O_5, TiO_2, Er_2O_3, La_2O_3, Pr_2O_3, Gd_2O_3, Y_2O_3, CeO_2 etc. and some of their silicates such as $Zr_xSi1_xO_y$, $Hf_xSi1_xO_y$, and $Al_xZr1_xO_2$ etc [5]. Some of these are discussed.

3.1 Aluminum oxide (Al_2O_3)

Al_2O_3 have high permittivity, high bandgap, high band discontinuities, and good break down voltage (see Table 1.1 [5]). But at the high processing temperatures (1000^o C) the mobility of electrons shows a flatband voltage shift in the positive direction. This shift could arise from either damage associated with gate electrode deposition or further processing steps [5].

3.2 Titanium dioxide (TiO_2)

TiO_2 has been used as an alternative gate dielectric material for deep submicron mosfet's earlier in 1995. The dielectric constant of TiO_2 is 80. The bandgap of the material is 3.5eV for amorphous films and 3.2eV for crystalline films. These band gaps are good for semiconductor but higher bandgap is required to act as an effective insulator. The TiO_2 has low energy band offset with respect to Si. TiO_2 has EOT of less than 10Å [5].

Transistors made with TiO_2 shows near ideal behavior but they have challenges with mobility. It has been shown that the low field effective mobility is approximately 160cm^2/V-s, which is about a three order lower than the mobility in SiO_2 based MOSFET's. This mobility reduction is due to interface trap state and surface roughness at TiO_2/Si interface. The electron traps in TiO_2 is due to oxygen vacancy. An empirical relationship between the effective mobility and the interface state density which is given by [5],

$$\frac{\mu}{\mu_o} = \frac{1}{1+\alpha D_{it}} \qquad (6)$$

Where D_{it} is the concentration of charged states at the bias condition and α is a constant. So the effective mobility is inversely related with D_{it} [5].

The strained-Si/high-k interface, the magnitude of the fixed charge is $10^{12}cm^2$. In Si/SiO_2 interface bond strain causes fixed charge which is about 0.1% of the interface atoms (10^{10}-$10^{11}cm^2$). So for strained-Si/TiO_2 leakage occurs from these defects as well as from low conduction band discontinuity.

Therefore, ultra-thin SiO_2 can be incorporated between TiO_2 and strained-Si layer to reduce the defect states at the interface [5].

Therefore if TiO_2 is grown on (100) Si substrate D_{it} decreases and the mobility increases. Mobility also can be increased by growing TiO_2 gate dielectric stack on Si substrate. The device speed can be improved by 20-80% at a constant gate length by using high mobility strained-Si at the channel region [5]. TiO_2 reduces gate leakage and Si enhances the device speed. Hence TiO_2 is our choice of high-k dielectric gate material.

3.3 Zirconium oxide (ZrO_2)

ZrO_2 is widely studied due to its dielectric constant (k~25) as well as higher band gap (~5.8Ev [5]). It is also thermodynamically stable with Si. However the crystallization temperature is about 500°C, which is low for ULSI processing. It has been reported that transition temperature that can be improved by adding impurities into the film of ZrO_2. This is because the dopant atoms distort the original ordered structure and therefore increase the entropy which in turn suppresses the crystallization process. Elements such Si, Al, and N is reported as effective dopant for this purpose. It has been, obtained 6–10Å EOT for ZrO_2 on the Ge p-MOSFET [5].

Table-3: High-k dielectric materials and their properties [5].

Gate dielectric Material	Dielectric constant (k)	Energy bandgap E_g (eV)	Conduction band offset ΔE_c (eV)	Valence band offset ΔE_c(eV)
SiO_2	3.9	9	3.5	4.4
Al_2O_3	8	8.8	3	4.7
TiO_2	80	3.5	1.1	1.3
ZrO_2	25	5.8	1.4	3.3
HfO_2	25	5.8	1.4	3.3
Ta_2O_5	25	6	1.5	3.4
Y_2O_3	13	6	2.3	2.6
Ya_2O_3	27	4.3	2.3	0.9

3.4 Hafnium oxide (HfO_2)

HfO_2 has been extensively studied due to its high dielectric constant and large energy band gap with high band offset as in table 1.1 [5]. It increases the EOT; belittles the high-k advantages. However, like ZrO_2, HfO_2 on Si substrate suffers from low crystallization temperature (~500°C). This crystallization temperature can be increased by incorporating Al_2O_3 with the HfO_2 ($Hf_xAl_{1-x}O_{1-y}$). There is an interfacial layer at $HfAl_2O_5$/Si interface which decreases the interface defects and eventually reduces the leakage current [5].

3.5 Yttrium oxide (Y_2O_3) and lanthanum oxide (La_2O_3)

Y_2O_3 is a good candidate for high-k dielectric oxide as it has higher band-gap of 6eV & and an energy band gap of 4.3eV as in table 1.1 [5]. Y_2O_3 has high dielectric constant 14-17 and good thermal stability up to 2325°C. Like Y_2O_3, La_2O_3 has relatively large dielectric constant ~18-30. But both of them have unwanted interfacial layer due to reaction with silicon. Moreover, they have highly intrinsic positive fixed charge that causes the mobility reduction [5].

3.6 Tantalum Pentoxide (Ta_2O_5)

Ta_2O_5 is a potential high-k candidate as it has high dielectric constant of 25 and reasonable band-gap of 4.4eV as in table 1.1 [5]. But due to poor thermal instability with Si and small electron band offset Ta_2O_5 is not popular for submicron MOSFET. But incorporation of Hf with Ta_2O_5 reduces the fixed charge density as well as leakage current. Addition of Zr with Ta_2O_5 increases the dielectric strength [5].

CONCLUSIONS

The decreasing sizes in metal oxide semiconductor (MOS) transistor technology require the replacement of SiO_2 with gate dielectrics that have a high dielectric constant (high-*k*). When the SiO_2 gate thickness is reduced below 1.4 nm, electron tunneling effects and high leakage currents occur which present serious obstacles for device reliability [1].

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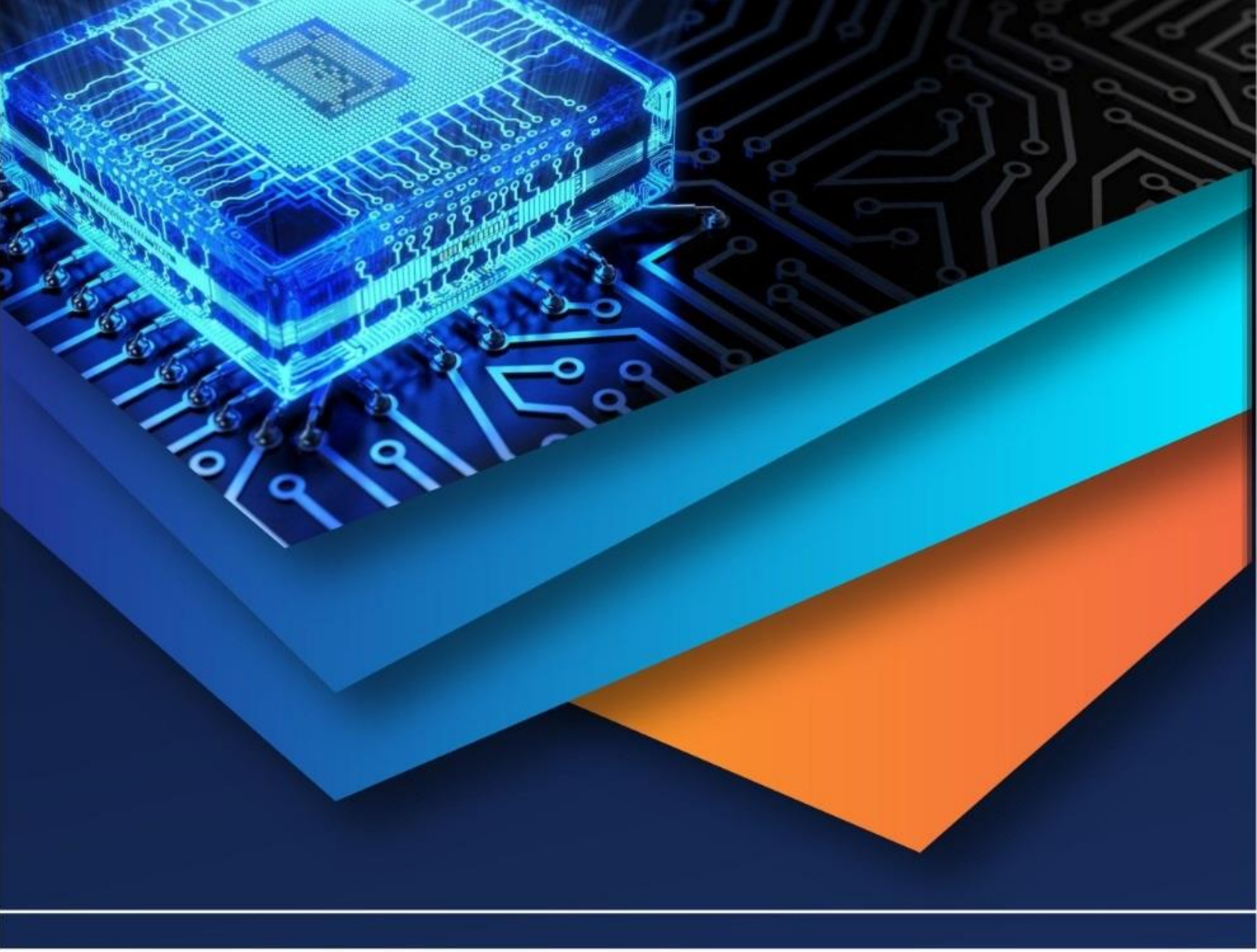

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