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Digital to Frequency Converting Flying Adder Architecture for Fractional Frequency Synthesis

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Abstract: ***Flying adder is an architecture which plays a vital role nowadays in our day to day life. It mainly helps to generate a fractional frequency from the given frequency. The main advantage in the architecture is it consist circuits which are pure digital. It can provide fast switching and reduce phase noise without effecting the phase locked loop bandwidth. Here Time average frequency concept is used , it makes clock generation easily. Combination of these two gives a Digital to frequency converter.***

Keywords: Flying adder, time average frequency, phase locked loop (PLL), Digital to frequency convertor.

I. INTRODUCTION

Flying adder is a digital circuit for example multiplexer, flip flops and accumulators. Nowadays digital circuits are widely used than analog because these analog circuits are sensitive to environment. Finally we will get corrupted signal. Better to use less number of analog components to get spectrally pure results. Previously we came across different PLL's example integer PLL, fractional PLL, sigma delta PLL. To generate direct frequency integer PLL is used. To fractional multiple of given frequency fractional PLL is used. These are facing a problem of spectrum purity degradation. Flying adder eliminates all these drawbacks without effecting loop bandwidth.

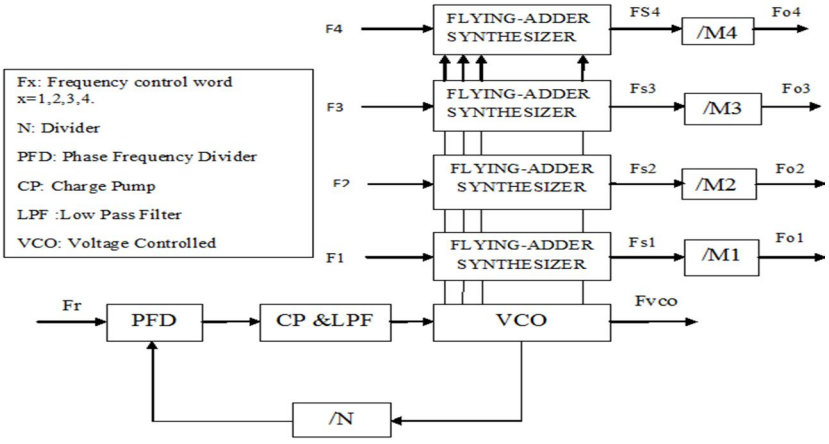

Fig . 1 ON-CHIP frequency generator using Flying adder's

II. FLYING ADDER AS ON-CHIP FREQUENCY GENERATOR

Direct period synthesis is also referred as Flying adder. Here Time average Frequency is used combination of these two concepts is known as digital to frequency convertor. By using this flying adder number of required PLL count in large circuits will reduce. For example consider only one PLL and take Flying adder's as many frequencies required as shown in fig .1 above.

III. FLYING ADDER ARCHITECTURE

Reference frequency is given to PLL from crystal oscillator. VCO present in PLL converts voltage to frequencies which are having same period with Δ phase difference. These VCO outputs are give as multiplexer input's as shown in fig.2 below .

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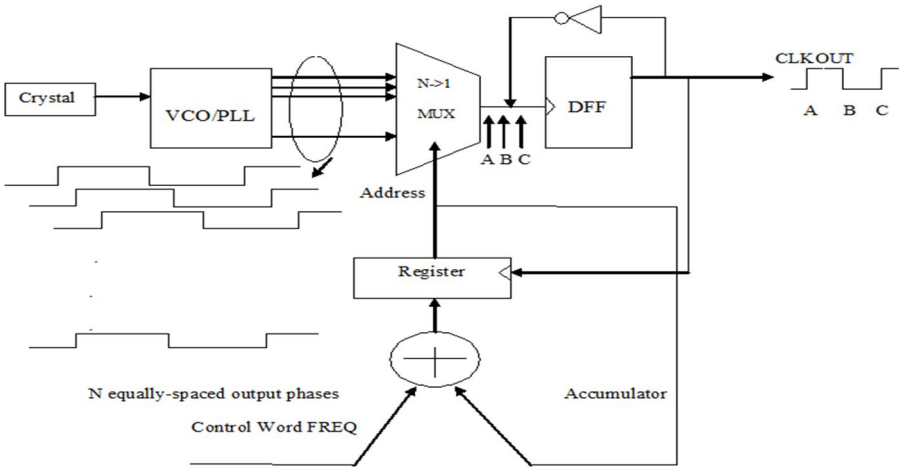

Fig .2 Flying adder architecture

Here we use accumulator and frequency control word which is fractional value given as input to it. According clock it accumulate the value. Only the integer sum value is given as selection line to multiplexer as shown in figure. Based on the selection lines multiplexer select one of it's inputs. Then multiplexer output is given as input for frequency divider then CLKOUT will be generated and it is given as clock for accumulator. Here accumulator, multiplexer and frequency divider comes ad flying adder it is completely digital generates spectrally pure signal.

IV. TIME AVERAGE FREQUENCY CONCEPT

Clock having same cycle length requirement completely made clock circuitry design complexity increases .In opposite way clock having different cycle length gives a direction towards Time Average Frequency concept from Frequency. Difference between these frequency and time average frequency is shown in fig .3 . In this case average frequency is considered .Average of the frequencies in a pattern as shown below

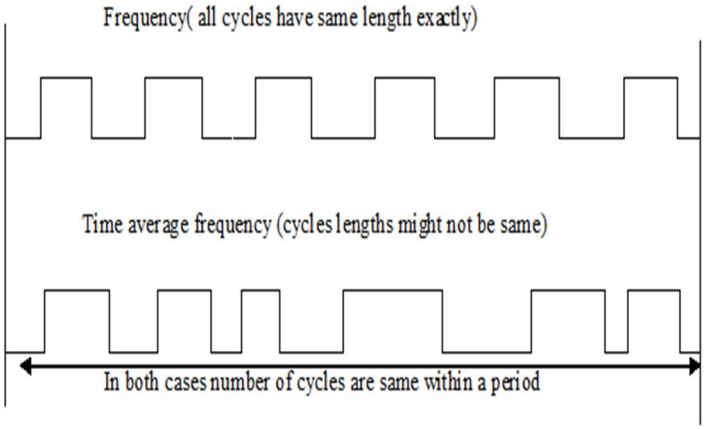

Fig. 3 Frequency and time average frequency difference.

V. FLYING ADDER WORKING PRINCIPLE

Let consider 5 bit frequency control word as 10 and its binary value is 01010b. K=32 inputs are given for multiplexer. The below block diagram fig .4 shows the working of flying adder. Initially value Mux address is 0 so 0 th input is selected as MUX out and it trigger's DFF . And then control word is added to it now address is 10 out of 32 inputs 10th input will be selected. Similarly 20th and 30th inputs are selected. Next 8th input is selected because Mux address crosses the limit 32. As shown in figure time between edges is 10Δ , therefore 20Δ is CLKOUT period.

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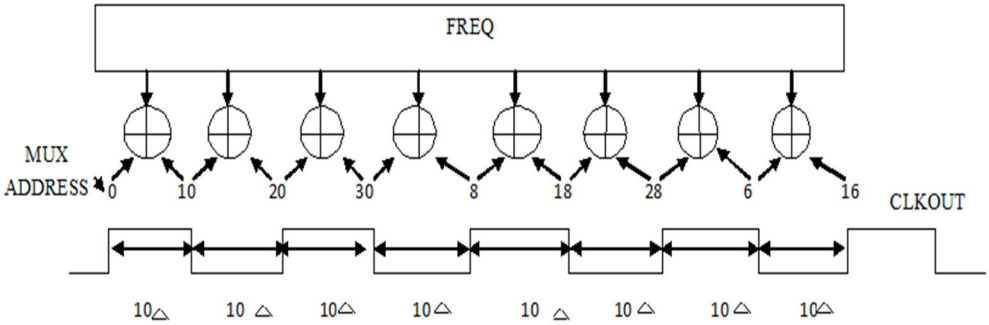

Fig .4 FREQ [4:0]=10=01010b and k=32 example for flying adder.

A. Forward Step

Here flying adder has fractional part also previously it has only integer part. Register having 5 bit integer part and 5 bit fractional part and it's operation is shown in below fig .5. Let consider 10 bit frequency control word as 10.25 and its binary value is 01010.01000b. K=32 inputs are given for multiplexer. The above block diagram shows the working of flying adder. Initially value Mux address is 0 so 0 th input is selected as MUX out and it trigger's DFF. And then control word is added to it now address is 10.25 out of 32 inputs 10th input will be selected. Similarly 20th and 30th inputs are selected.

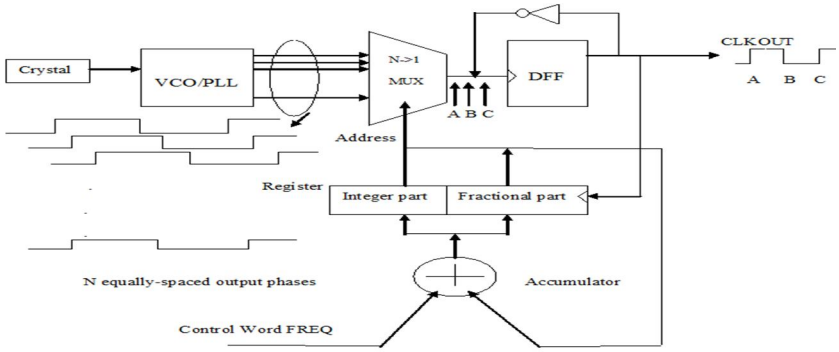

Fig 5. Flying adder architecture

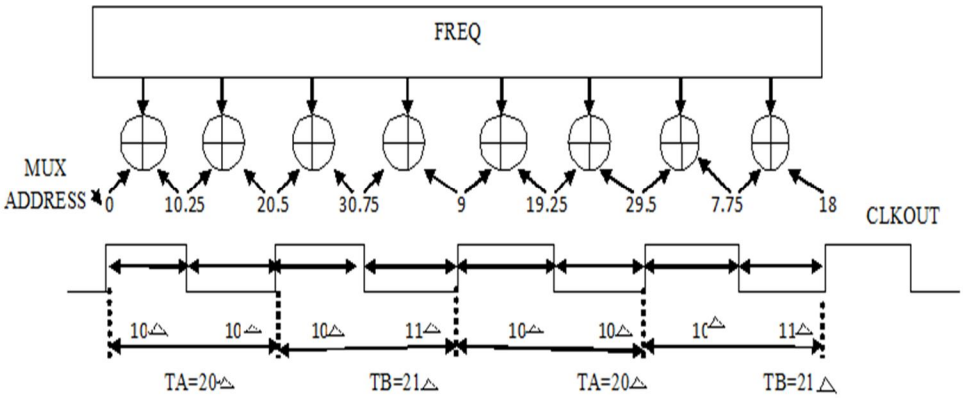

Fig. 6 FREQ[9:0]= 10.25 =01010.01000b and k=32 example for flying adder

Next 9th input is selected instead of 8th as in above case. So the clock which is synthesised gets one more Δ. By this fractional part cycle prolonging takes place. As shown in fig .6 it have different time period TA= 20Δ and TB= 21Δ consecutively like ABABAAB pattern. Here Time average frequency concept will plays an important role. Now fundamental frequency = (20Δ+21Δ)= 41Δ and the average frequency is T_{TAF}= (41Δ)/2 = 20.5Δ .By changing the fractional part we can observe different patterns and cycle prolonging also takes place differently this concept is very helpful to generate different frequencies.

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B. Digital To Frequency Convertor

By these flying adder and time average frequency techniques a new component digital to frequency converter (DFC) comes into role. And it is shown in below fig. 7.

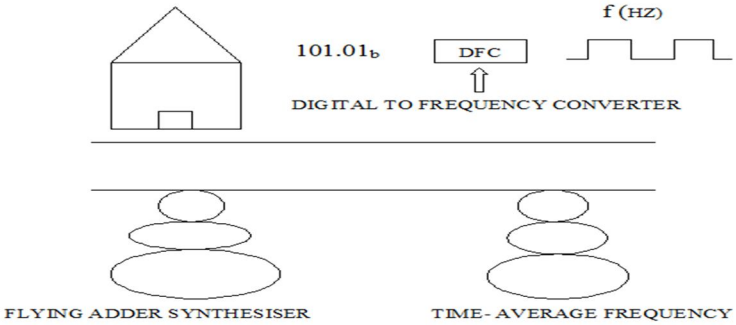

Fig 7. Digital to frequency converter

C. Output waveform:

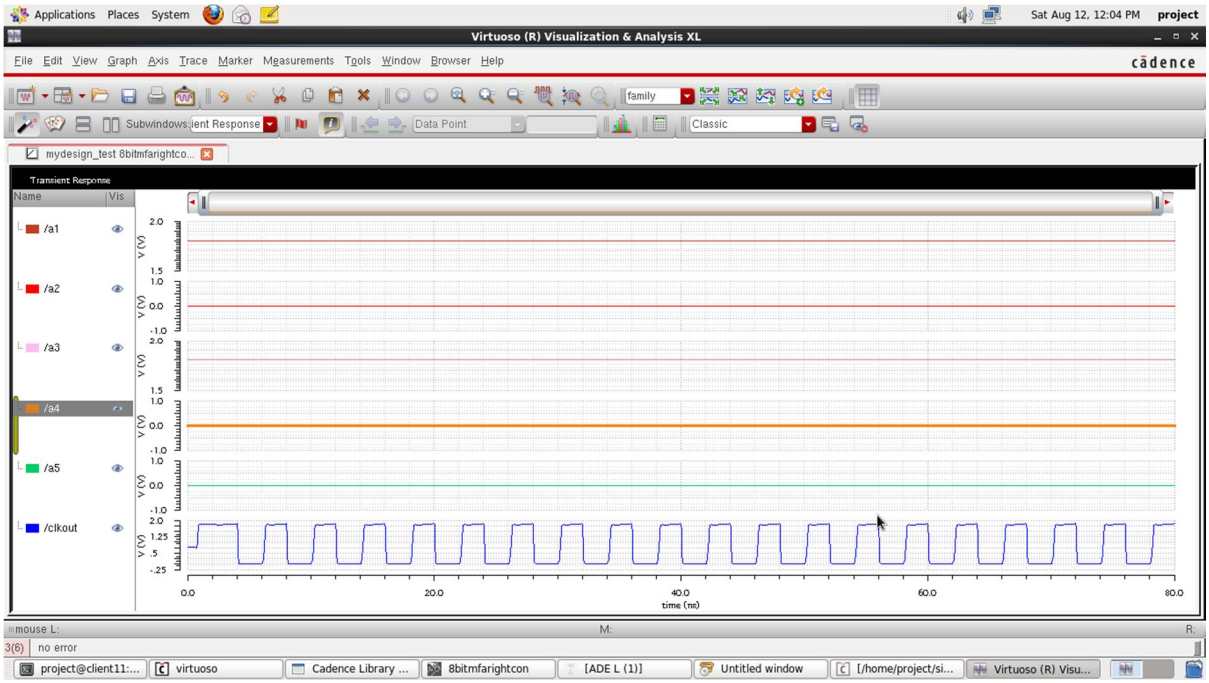

Fig 9. Digital inputs and it's frequency output

D. Results

Control word A=101.00=>5 , carry-in CIN=0 , delay between two VCO signals Δ=0.401ns

1) Theoretical Value

Time delay between two adjacent outputs

output clock = control word ×Δ×2

=5 × 0.401n × 2

=4.01ns

Desired output clock freq=1/4.01ns=249.37Mhz

2) Practical Value

Output clock freq =245.4Mhz

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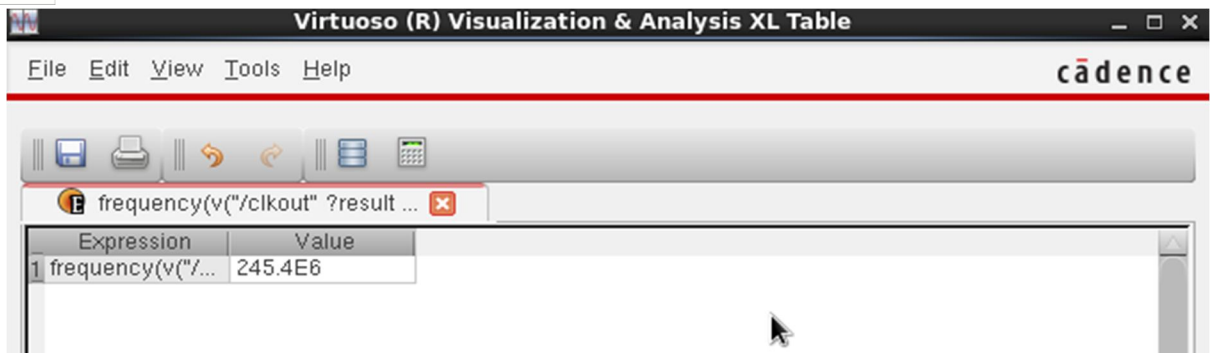

VI. CONCLUSION

B y these flying adder and time average frequency techniques a new component digital to frequency converter (DFC) comes into role. This technique is useful to get generate fractional frequencies very easily without facing difficulties like environmental changes as it is completely consist of digital circuits. This proposed technique improves frequency switching and phase noise. For generating large systems ON-CHIP frequencies this flying adder helps a lot to reduce area.

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