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TSOP And TSON Testability Analysis And Realizations Of Domino VLSI CMOS Logic

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Abstract: ***The design for TSOP and TSON fault testability analysis and realizations of Domino VLSI CMOS Logic has been proposed. Domino VLSI CMOS circuits are fast dynamic CMOS circuits and hence suitable for fast and critical circuit applications. The proposed design beat the charge sharing difficulty with enhanced testability using faults TSOP and TSON. Furthermore, increase in number of transistors in the circuits, the proposed scheme shows uninterrupted power decrement in contrast to other schemes.***

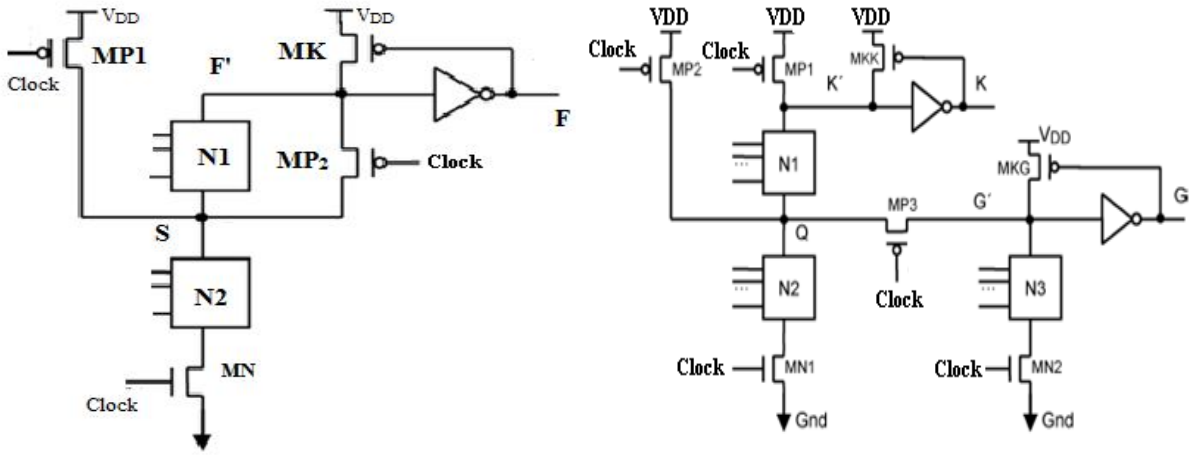
Keywords: Domino, Testability, Precharge, TSOP and TSON

I. INTRODUCTION

Domino logic , with faster switching speed and required less silicon area. Hence, characteristic [1-4] of Domino circuits have been used in high performance critical circuits like microprocessors [5-7]. Dynamic CMOS logic has more advantage in terms of testability. The natural problem with Domino CMOS circuit, it suffer from noise margin trouble. Due to charge redistribution between parasitic capacitances at the internal nodes of the circuit gives false output. [8]. Domino logic has single clock used to precharge the dynamic node during precharge phase in NMOS network. When Clock = 0 the dynamic node is charged to logic 1 through the PMOS MCP. Output is discharged to logic 0. When clock is = 1 problem may be evaluated through the PDN. For the period of evaluation phase, transition of node F (F') can be 0 or 1. Depending on the input conditions in evaluation phase, Dynamic node F,`if left floating PDN is in open state, hence charge leakage from dynamic node F` due to leakage currents. Keeper transistors are used to avoid this problem. [9-10].

II. LITERATURE REVIEW

TSOP and TSON testability problem, for the secondary precharge transistors, to put them on a chain from V_{DD}, passes through all inner node, be precharged, and ends at the output of the dynamic gate, in Figure 1(a) & (b)



(a) (b)

Figure 1(a) & (b).**:** Reported testable Domino Circuit.

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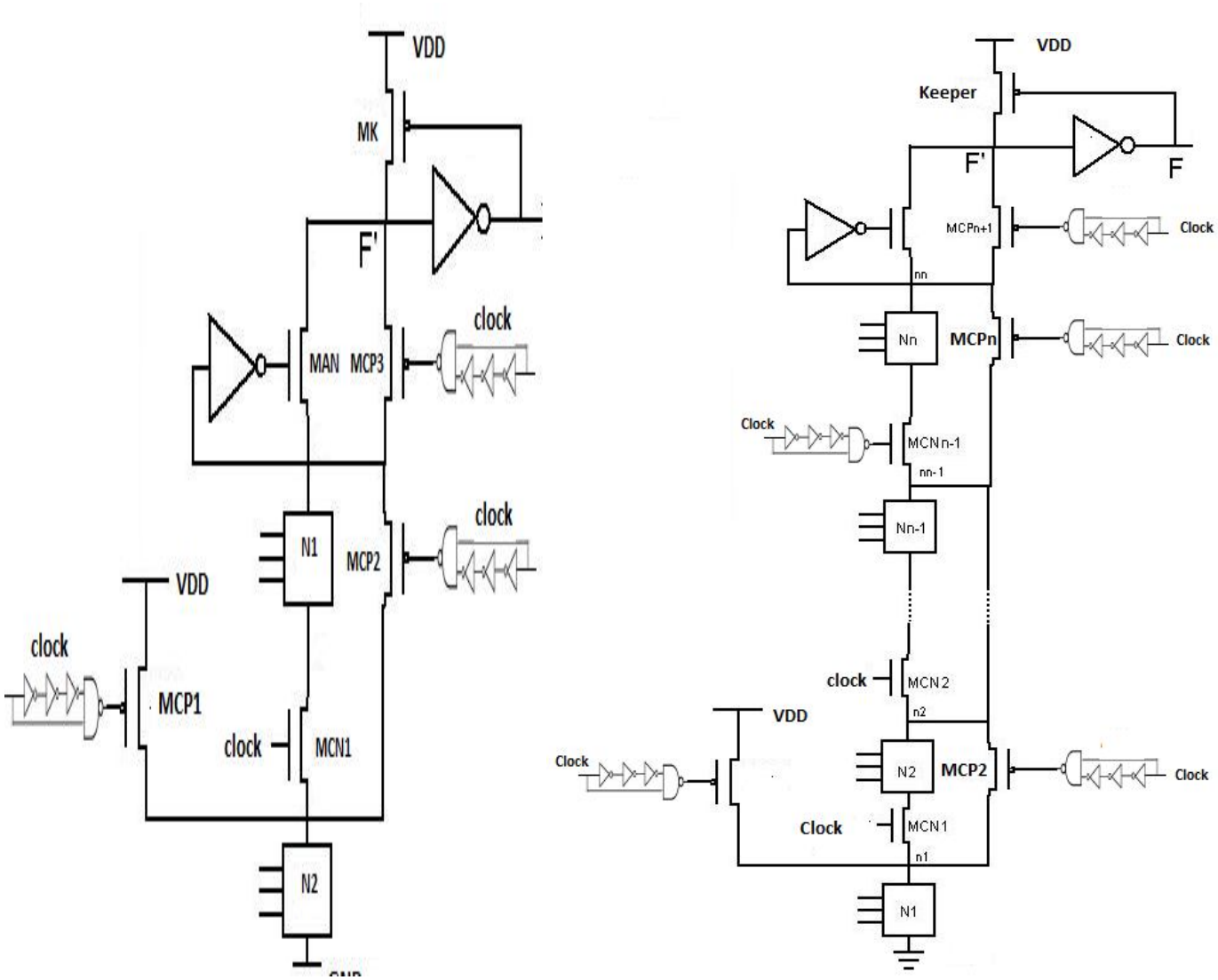
III. PROPOSED WORK

A TSOP and TSON fault, testability analysis technique has been proposed to overcome the fault detection problem associated with the secondary precharge transistors. Hence numbers of PMOS transistors from V_{DD}, through critical internal nodes and ends at the node F'. Also change the position of clocked NMOS (Figure 2 (a) & (b)) and placed between NMOS blocks. Add one activation MAN with one inverter in the logic.



(a) (b)

Figure 2 (a) & (b) Modified testable Domino Circuit .

IV. SIMULATION RESULT

The following parameters performance are evaluated Power dissipation, Propagation delay and power- delay product using Synopsys HSpice. using 0.18-µm CMOS VLSI technology for Design Testability [11-12]. The Power, Energy and Delay calculation for various configurations are shown in Table I to Table VI.

Table I : Power & Energy (Equal Size Transistors)

Type/Size	2	3	4	5	6	7	8	9	10
Stnd.M. Power	22.1µ	26.7µ	31.8µ	36.5µ	41.2µ	46.7µ	49.3µ	55.7µ	60.3µ
I Power	24.7 µ	29.6 µ	33.6 µ	38.3 µ	43.5 µ	47.1 µ	52.9 µ	55.3 µ	58.9 µ
II Power	38.5 µ	36.4 µ	49.8 µ	55.4 µ	61.8 µ	67.5 µ	73.8 µ	79.2 µ	86.3 µ
Prop. Sch. Power	25.1 µ	26.2 µ	30.9 µ	32.2 µ	35.1 µ	37.2 µ	40.2 µ	42.9 µ	45.7 µ
Stnd.M. Energy	1.77f	2.33f	3.1f	3.97f	4.66f	5.89f	6.64f	8.16f	9.35f
I Energy	3.16f	4.30f	5.41f	6.73f	8.02f	9.7f	11.2f	11.7f	14.1f
II. Energy	4.03f	4.4f	6.11f	7.36f	8. 2f	10.1f	11.8f	13.8f	15.1f
Prop. Sch. Energy	3.21f	3.2f	3.44f	3.90f	4.34f	4.35f	5.14f	5.08f	6.10f

Table II: Delay (Equal Size Transistors)

Type/Size	2	3	4	5	6	7	8	9	10
Std.Multi.Delay	86p	97p	104p	117p	123p	135p	141p	155p	161p
I Delay	131p	143p	158p	172p	186p	208p	219p	232p	246p
II Delay	106p	125p	127p	135p	144p	157p	167p	181p	188p
Prop. Sch. Delay	131p	121p	122p	125p	130p	131p	141p	142p	144p

Table III: Power & Energy (Equal Energy Design)

Type/Size	2	3	4	5	6	7	8	9	10
I Power	24.8µ	28.9µ	33.1µ	38.2µ	42.4µ	46.8µ	53.7µ	54.5µ	58.9µ
II Power	38.3µ	43.6µ	49.8µ	54.9µ	52.5µ	66.6µ	72.9µ	78.8µ	84.2µ
Prop. Sch. Power	25.7µ	26.9µ	28.9µ	31.8µ	32.9µ	35.6µ	37.5µ	39.9µ	42.2µ
1. Energy	3.39f	4.54f	5.67f	6.89f	8.78f	9.89f	12.03f	12.7f	14.8f
2 energy	3.83f	4.89f	6.09f	7.32f	7.38f	10.2f	11.54f	13.43f	15.7f
Prop. Sch. Energy	3.48f	3.19f	3.61f	3.92f	4.16f	4.66f	4.93f	5.47f	5.89f

Table IV: Delay (Equal Energy Design)

Type/Size	2	3	4	5	6	7	8	9	10
I Delay	129p	145p	159p	172p	190p	205p	218p	231p	243p
II Delay	101p	111p	119p	128p	140p	151p	162p	172p	183p
Prop. Sch. Delay	133p	117p	124p	126p	128p	132p	133p	138p	139p

Table V: Power & Energy (Equal Evaluation Design)

Type/Size	2	3	4	5	6	7	8	9	10
I Power	24.1µ	29.3µ	33.6µ	37.3µ	41.2µ	46.1µ	48.4µ	53.1µ	57.3µ
II Power	37.9µ	42.6µ	47.9µ	53.4µ	60.1µ	65.2µ	70.9µ	77.2µ	82.1µ
Prop. Sch. Power	25.1µ	27.3µ	30.3µ	31.4µ	35.9µ	38.2µ	42.7µ	44.2µ	48.7µ
I Energy	3.07f	4.00f	5.03f	6.15f	7.11f	8.56f	10.12f	11.6f	12.8f
II Energy	3.75f	4.82f	5.47f	6.89f	8.40f	9.67f	10.8f	12.6f	13.7f
Prop. Sch. Energy	3.21f	3.11f	3.25f	4.24f	4.43f	4.9f	5.23f	6.13f	6.83f

Table VI: Delay (Equal Evaluation Design)

Type/Size	2	3	4	5	6	7	8	9	10
I Delay	125p	133p	154p	162p	171p	189p	202p	210p	229p
II Delay	102p	103p	113p	120p	133p	141p	148p	159p	168p
Prop. Sch. Delay	128p	120p	121p	123p	128p	129p	131p	138p	142p

V. CONCLUSION

The design for TSOP and TSON testability analysis and realizations of Domino CMOS Logic has been proposed. Domino CMOS circuits are dynamic and hence suitable for fast and critical circuit applications. Possible extensions to proposed design reduce the charge sharing difficulty with enhanced testability using faults TSOP and TSON but separate algorithm to optimize delay under a power constraint. Furthermore increase in number of transistors in the circuits the proposed scheme shows uninterrupted power decrement in contrast to other schemes.

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