International Journal for Research in Applied Science & Engineering Technology (IJRASET)
ISSN: 2321-9653; IC Value: 45.98; SJ Impact Factor:6.887
Volume 5 Issue IX, September 2017- Available at www.ijraset.com

A Modified High Hysteresis Low Power CMOS Schmitt Trigger

Chanchal Chawla[1], Bhavana Dhull[2],
[1, 2] *Department of Electronics & Communication, B.P.I.T, I.P University GGSIPU, Delhi, India*

Abstract: This paper describes a new Schmitt trigger for getting wide hysteresis to improve noise margin as compared to conventional Schmitt trigger. Schmitt trigger is an electronic circuit that converts any analog signal to digital signal. This bi-stable circuit in which there is an output transition from low to high and high to low voltage will occur at different thresholds shows hysteresis. In designed Schmitt trigger hysteresis width is improved by using two feedback loops. The results are compared with conventional CMOS Schmitt trigger at different voltages. Schmitt triggers have been realized using .25 µm and .18µm CMOS technology.

Keywords: hysteresis width, static power dissipation, dynamic power dissipation

I. INTRODUCTION

Schmitt trigger is a bistable network, a circuit that is widely used to improve noise immunity and interference. As a noise suppressor it works very good. Schmitt's Trigger uses the waveform, therefore it is widely used to convert analog signals into digital signals, and re-forming a rough rectangular pulse or twist. Hysteresis trigger eliminate noise, resulting in a cleaner and more reliable signal. When the trigger point by the front input voltage (UTP), when the trigger point voltage through a negative input, the output of the Schmitt flip-flop to change state. Conventional fixed Schmitt trigger having a hysteresis width [1].

This article describes how to use the two feedbacks to increase the hysteresis width of the conventional Schmitt trigger device. Second section describes the general design of the Schmitt trigger. In the third part, the description will be described with an adjustable Schmitt trigger circuit to increase the hysteresis width. In section IV comparison between conventional Schmitt trigger and new designed Schmitt trigger on the basis of hysteresis width and power dissipation in terms of static and dynamic is discussed. These circuits are made using standard CMOS technology. The results can be found in section IV.

II. DESIGN OF CONVENTIONAL CMOS SCHMITT TRIGGER

In this section, discussion is done on dc as well as transient analysis of Schmitt trigger. [2] This section also emphasize on the effects of W / L on the hysteresis curve.

Schmitt circuit is a common inverter circuit (two-transistor inverter), having two transistors that provide additional hysteresis. The double transistor inverter is used because the transistors (M2 and M5) have higher threshold voltage than M1 and M4 due to body bias effect, which leads the output to switch to high from low or low from high when M2 and M4 are in ON condition.

The addition of transistors M6 and M3 generates hysteresis. When input voltage applied to the terminal M1 and M2 is 0v, both the transistors operate in cut off mode. As a result both are in off condition. Transistors M4 and M5 are in on condition that raise the output voltage to logic high level.

When the input reaches the threshold voltage of the transistor M1, the M1 is turned on, while M2 is closed, then the high output turns on M3. Current starts flowing through M3. The node between M1and M2 is pull down by transistor M1. The on transistor M3 tries to pull up this node voltage to VDD-VT. The transistor M2 is maintained at a high logic level output. When the input voltage exceeds the threshold M2, the output is switched to a low logic level. As a result the switching point is switched to a higher voltage, called VIH.

When input falls from higher logic level to lower logic level, PMOS's is responsible for shifting the switching point to VIL(lower voltage level). The difference between the VIH and VIL is referred as HYSTERISIS voltage i.e. the amount of voltage to be added to low logic level at output or is to be subtracted from high logic level at output, logic level at the output will remain same.

If we examine the conditions from transistors (M1, M2, M3).

When output switches from high to low just before that:

M2 in off condition. M1 and M3 in saturation condition.

$$I_{DM3} = \beta_3/2(V_{GS} - V_{TH3})^2$$

$$= \beta_3/2(V_{DD} - (V_{in} - V_{TH2}) - V_{TH3})^2$$

$$= \beta_3/2(V_{DD} - V_{in} + V_{TH2} - V_{TH3})^2$$

But $V_{TH2} = V_{TH3}$

$$I_{DM3} = \beta_3/2(V_{DD} - V_{in})^2$$

$$I_{DM1} = \beta_1/2(V_{GS} - V_{TH1})^2$$

$$= \beta_1/2(V_{in} - V_{TH1})^2$$

$I_{DM1} = I_{DM3}$ (Both are in saturation)

$$\beta_3/2(V_{DD} - V_{in})^2 = \beta_1/2(V_{in} - V_{TH1})^2$$

$$V_{DD} - V_{in} = \sqrt{\beta_1/\beta_3}\,(V_{in} - V_{TH1})$$

$$V_{in} = \left[V_{DD} + \left\{\sqrt{(\beta_1/\beta_3)}\right\}V_{TH1}\right] \Big/ \left\{1 + \sqrt{\beta_1/\beta_3}\right\}$$

This Vin is called VIH. Now Similarly for the VIL.

Transistors M4 and M6, will be in saturation.

$$I_{DM6} = \beta_6/2(V_{SG} - |V_{TH6}|)^2$$

$$= \beta_6/2(0 - (V_{in} - V_{TH5}) - V_{TH6})^2$$

But $V_{TH5} = V_{TH6}$

$$= \beta_6/2(V_{in})^2$$

$$I_{DM4} = \beta_4/2(V_{SG} - |V_{TH4}|)^2$$

$$= \beta_4/2(V_{in} - V_{DD} - V_{TH4})^2$$

$I_{DM4} = I_{DM6}$ (Both are in saturation)

$$\beta_6/2(V_{in})^2 = \beta_4/2(V_{in} - V_{DD} - V_{TH4})^2$$

$$V_{in} = \sqrt{(\beta_4/\beta_6)}\,(V_{DD} - |V_{TH4}|) \Big/ 1 + \sqrt{(\beta_4/\beta_6)}$$

This V_{in} is called V_{IL}

The circuit designed for V_{IL} = 2V and V_{IH} =3 is shown in Fig. 1. And results are shown in Fig. 2 and Fig.3

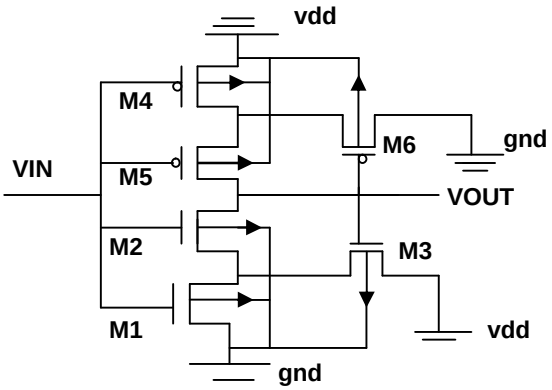

Fig.1 Conventional CMOS Schmitt Trigger

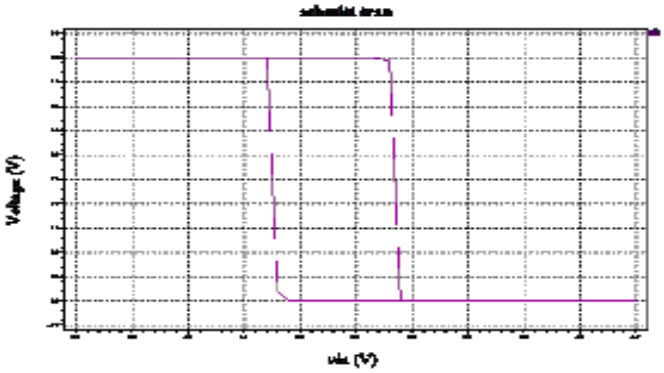

Fig. 2 DC Analysis

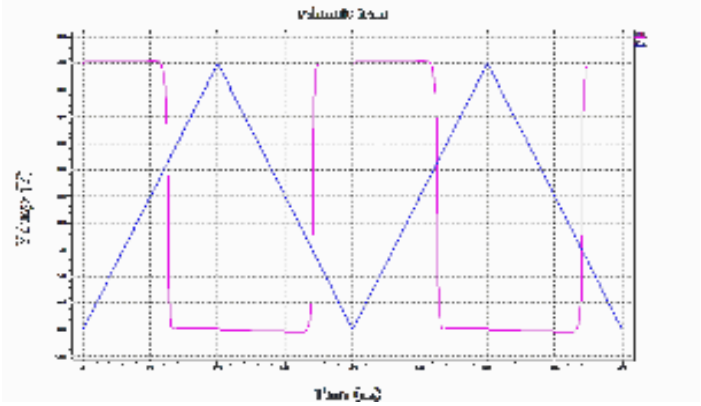

Fig. 3 Transient Analysis

A. Effect of Variation of W/L ratio of transistors on Hysteresis Curve

On increasing the W/L of transistor M1 the curve will shift towards the LEFT side, because in this case our NMOS will strong and pulls the output sharply to low logic level. Second case when M4 will strong then it will maintain the output to logic level high for greater duration so the curve will shift to RIGHT side. There will no effect on the hysteresis curve on changing the sizes of transistors M2 and M5. This can be also verified from the equations derived for VIH and VIL in previous section.If the size of transistor M3 is increased then it will affect only on VIH level, because when we increase from low to high then lower portion of SCHMITT comes into picture to control the VIH level, hence by increasing the size the VIH will increase while in same way transistor M6 affect only on VIL level. When size of M6 is increased then VIL will be reduced. We can also conclude that the aspect ratio of M4 and M4 transistors affect the VIL level while the aspect ratio of M1 and M3 affect the VIH level. The area of hysteresis curve determines the amount of noise immunity provided be the circuit. Greater the difference between the VIH and VIL level means more immunity. Hysteresis width of conventional CMOS Schmitt trigger is increased by new circuit which consist of two layers of feedback devices . This new circuit will be discussed in the next section. The effect of varying W/L is shown in Figure 4

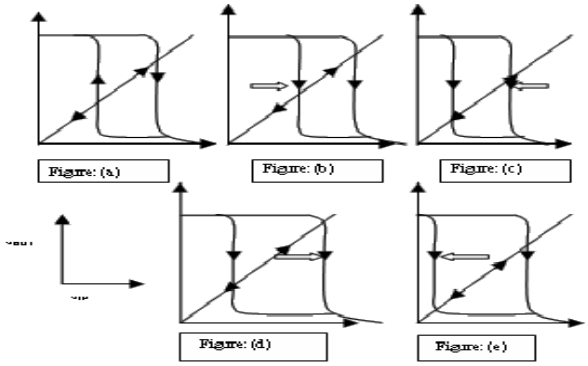

Figure 4 Effect of W/L ratio of various transistors on Hysteresis Curve.

1) Typical case b) When W/L of M4 increases c) When W/L of M1 increase
2) When W/L of M3 increase e) when W/L of M6 increase

III. CIRCUIT TO IMPROVE THE HYSTERESIS WIDTH

Large hysteresis width can be achieved with two layers of feedback devices for both VIH and VIL trigger edges. Design considerations are almost same as in conventional Schmitt trigger. Hence higher VIH and lower VIL can be achieved by two layers of feedback devices [4]. The circuit is shown in Fig 5. And transient analysis is shown in Fig. 6

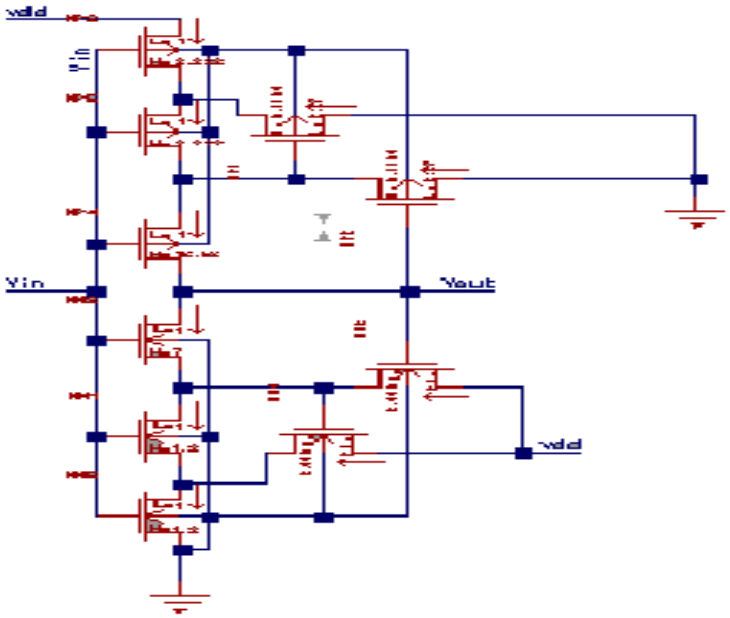

Fig. 5 New circuit to improve hysteresis width

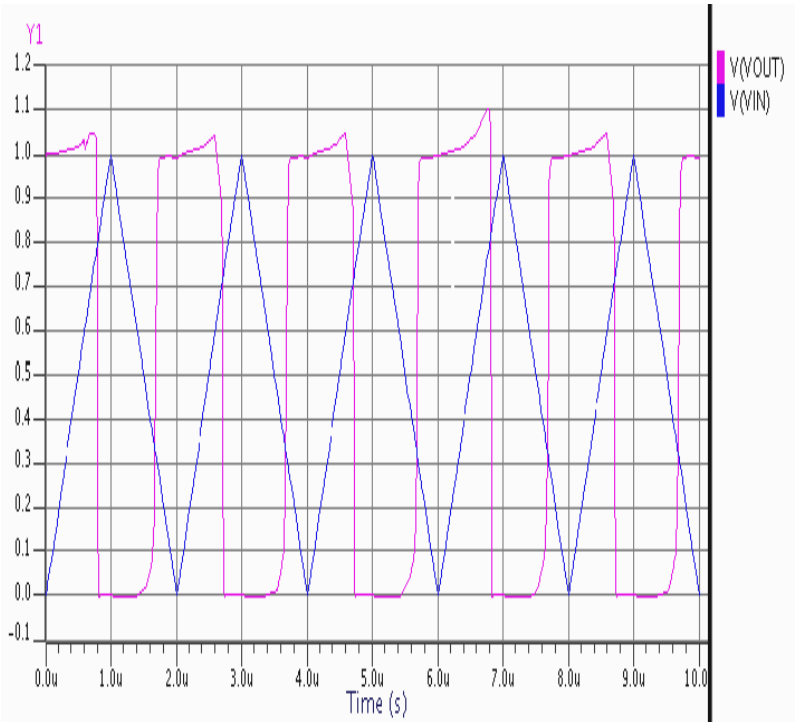

Fig. 6 Transient analysis of new circuit at 1V

Transient analysis of conventional Schmitt trigger at 1V is shown in Fig.7

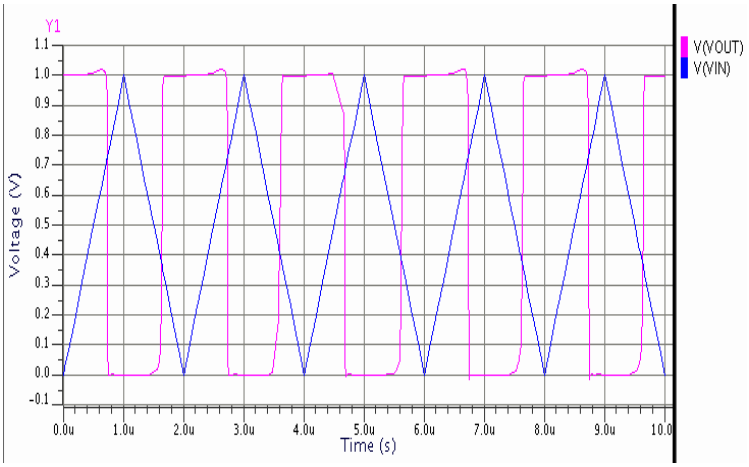

Fig: 7 Transient analysis of conventional Schmitt trigger at 1V

IV. SIMULATION RESULTS

For the simulation of conventional and new circuit BSIMV3 Ver 3.1 models of TSMC 0.18µm CMOS process were used. Tanner tool with 0.25µm CMOS process were also used to compare the hysteresis width and average power consumed of conventional and new Schmitt trigger circuits. Simulations results are reported in Table 1 and Table 2. These results show that high hysteresis width is achieved with modified Schmitt Trigger.

Voltage (V)	Hysteresis width Old/new circuit	Dynamic power dissipation Old/new (nW)	Static power dissipation Old/new (pW)
0.8	0.33/0.45	245.4 / 297.952	11 / 25.8
0.9	0.33/0.45	392.6664 / 555.273	13 /29.7
1.0	0.33/.5	612.7 / 729.63	15 /23.8
5	1/2	0.5550 / 0.585	215.187 / 452.3

Table 1. Comparison between hysteresis width, static power dissipation, and dynamic power dissipation.

Voltage (Volt)	Hysteresis Width (Volt) Old / New	Average Power Consumed (watts)
5V	1.2 / 2.1	7.999 e – 004 / 3.930 e – 004
3V	0.8 / 1.3	2.4499 e – 004 / 8.0565 e – 004
1.5V	0.4 / 0.85	1.08310 e – 004 / 1.1150 e – 004

Table 2. Comparison between hysteresis width and average power consumed.

V. CONCLUSION

The new Schmitt trigger provides larger hysteresis width as compared to conventional Schmitt trigger. The dynamic power dissipation is almost comparable but static power dissipation of new circuit is almost double as compared to conventional one. This circuit is useful where we require large hysteresis width to improve noise margin.

REFERENCES

[1] CMOS digital integrated circuits: analysis and design By Sung-Mo Kang, Yusuf Leblebici
[2] CMOS: circuit design, layout, and simulation, Volume 1 By R. Jacob Baker
[3] J. P. Uyemura, Circuit Design for CMOS VLSI.
[4] C. T. Chuang and J. B. Kuang, "SOI CMOS Schmitt trigger circuits with controllable hysteresis," U.S. Patent 6 441 663, Aug. 27, 2002
[5] Pfister, A. Novel CMOS Schmitt trigger with controllable hysteresis. IEE Electronics Letters, 28(7), 639–641, (1992).
[6] IEEE Transactions On Circuits And Systems-1: Fundamental Theory And Applications, Vol. 41. No. 1, January 1994Dokic, B. L.: 'CMOS Schmitt triggers', IEE Proc. G, 1984, 131, (5), pp. 197-202