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Certificate

It is here by certified that the paper ID : IJRASET13369, entitled

Design and Operational Synthesis of 64-bit Adder and Subtracter Unit using Delay Efficient Parallel Prefix Technique

by

Akash Tiwari

after review is found suitable and has been published in Volume 6, Issue I, January 2018

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Good luck for your future endeavors

Editor in Chief, iJRASET