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Design and Performance Comparison of 16-Bit UT Multiplier using Reversible Logic

K. Yogeswari

after review is found suitable and has been published in

Volume 7, Issue IV, April 2019

in

It is here by certified that the paper ID : IJRASET21521, entitled



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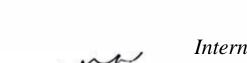
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