



ISSN No. : 2321-9653

# iJRASET

International Journal for Research in Applied  
Science & Engineering Technology

iJRASET is indexed with Crossref for DOI-DOI : 10.22214

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*VLSI Architecture of Encoding using Sols Technique for Reducing Power in DSRC*

*by*

*K. Rathna Sree*

*after review is found suitable and has been published in*

*Volume 8, Issue VI, June 2020*

*in*

*International Journal for Research in Applied Science &  
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