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*It is here by certified that the paper ID : IJRASET50158, entitled  
A Low Power 10T SRAM Cell with Extended Static Noise Margins is Used to  
Implement an 8 by 8 SRAM Array in 16nm CMOS*

*by*

*T. Venkata Lakshmi*

*after review is found suitable and has been published in  
Volume 11, Issue IV, April 2023  
in*

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